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EXAMINER	
HO, THOMAS M	

ART UNIT	PAPER NUMBER
2134	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/672,368	MCKEEN ET AL.	
	Examiner	Art Unit	
	Thomas M. Ho	2134	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *07 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 are pending.

2. The amendment of 6/7/05 has been received and entered.

Response to Arguments

The Applicant has observed that the Examiner has cited a new reference, and has issued a rejection upon claim 9 for the same reasons as claim 5. Accordingly, the Applicant has argued that the finality of the current office action is premature. The Examiner has fully considered Applicant's arguments and found it persuasive. Accordingly the finality of the previous action is withdrawn.

Applicant has argued the following with regards to claim 1:

"Applicants believe that the Examiner has identified a distinction without a difference: as the Examiner is clearly aware, each process executing on a machine typically has its own page table, but some contents of the table may be partially shared (as for example, when two processes share pages). However, two such processes, either with or without shared pages mapped into their virtual address spaces, do not execute in any distinguishable different mode instead.."

The Examiner however contends that the Applicant own invention does not appear to distinguish between the isolated execution mode and the normal execution mode in any manner than is more substantial than disclosed by the processes of Coulouris. The Applicant's own invention appears to only distinguish between two modes of execution by the handling of asynchronous events in different environments, such environments being defined by a memory map, and the respective class of events that the sequence of execution for a particular memory map is supposed to handle.

"...their address spaces are isolated (or not) solely as a result of the contents of their respective page tables. In other words, any difference in the way the processes execute is a result of the different page tables, and not a cause of the use of one page table over another. For at least these reasons, Applicant's respectfully submit that the references of record fail to teach or suggest at least the normal and isolated execution modes as recited in claim 1, and ask that the Examiner withdraw the rejections of the claim."

Applicant appears to argue that because the address spaces are isolated as a result of their page tables, the differences in the way the processes execute is a result of the different page tables and not through cause of using one page table over another.

The Examiner contends that how the address spaces are isolated even if it is the result of the contents of respective page tables is irrelevant to the rejection at hand. Indeed, as the Applicant has stated, one of the ways in which the address spaces are isolated come about as a result of the

different contents of their respective page tables. However, this does not preclude the fact that a different mode of execution may come about by these different contents. The Examiner previously argued that events that are to be handled by the code in one process are handled by that process, while events that are to be handled by the code of another, are handled by another. The executing code between each process is swapped in an out depending on the nature of the interrupt. For Example, suppose the Examiner was running two processes on his computer. One process detects mouse movements, while another process is listening to a port. Both of these events are asynchronous events. The computer's operating system event handler will switch the code the CPU is currently executing to the code of the process designated to handle the mouse motions. If information appears upon the port the other process is listening to however, the operating system will again switch the mode of execution to the code which exists in the memory map of the other process to handle the data received on the port.

Thus the Examiner agrees with Applicant's following statement "*In other words, any difference in the way the processes execute is a result of the different page tables...*" but disagrees with the Applicant's conclusion "*and not a cause of the use of one page table over another.*" Given how a set of processes is structured, these two items are not mutually exclusive.

Applicant has not argued the individual claim limitations of claim 1 but appears to have argued the ideological nature as a whole as to whether or not processes can teach or suggest isolated execution modes. The Examiner believes these arguments have been addressed.

In reference to claim 5, Applicant has argued:

"However, Applicants believe that the only common element between these two operations is the name "mirroring." In the RAID context, identical data is placed on two physical devices, so that if one of the devices fail, the data can be recovered from the other. By contrast "mirroring" in claim 5 refers to maintaining two page table base address registers, of which one is selected based on a signal which indicates one of normal or isolated execution mode. Apart from the name, Applicants can find little commonality between RAID mirroring and mirroring a page table base address register.

Applicant appears to once again apply a unique and unusual attack on the ideological basis of the Examiner's rejection. However, the Examiner contends that whether a table base address register is being mirrored, or a hard drive is being mirrored, the basic principle remains the same. Mirroring is a technique in which a copy of one piece of data is resident on typically two or more accessible mediums. Mirroring with respect to Internet sites, refers to the identical internet site being accessible from another website location. Mirroring with respect to hard drives refers to the duplication of the data of one hard drive onto another. Often times, but not always, this is arranged such that any change to one hard drive will result to a change in its mirror. The advantage of such a method is that, the data is accessible by more than one means, speeding up the accessibility of the data. For this reason, the Examiner's maintains the rejection of claim 5.

The Examiner also maintains the rejection of claim 5 for an additional reason. It is evident that a hard drive stores all the data of a computer system, including the operating system. For this reason, the Examiner has noted in the previous action that the relied upon section of Silberschatz discloses that memory maps, page taps, and processes may be placed on the hard disk itself in virtual memory. In this way, mirroring of the entire hard disk would necessarily disclose mirroring of the page table maps and address registers as this information would be apart of the operating system on the hard drive, though it is not explicitly stated.

Applicants additional arguments appear to be a repeat of the previously presented arguments, as the Examiner has formerly rejected the later claims with the same basis as the previous claims.

With respect to claim 2, it would indeed appear that the Examiner neglected to illuminate a proper disposition with regards to the previous amendment made by the Applicant. However, the finality of the previous action has been withdrawn in light of this fact, and with respect to claim 9.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coulouris et al. and Silberschatz et al.

In reference to claim 1:

(Coulouris et al. Section 6.3 Processes and Threads) discloses a method comprising:

- Identifying if an event is one of a class of events to be handled in the isolated execution mode, where the isolated execution mode is a processor running a secure process (Page 168), and the event is one of an event or events that might be handled by that process, where threads within a process have their own software interrupt handling mechanisms
- Handling the event using the first page table map if the event is identified as one of the class of events to be handled by the isolated execution mode, where the first page table map is the virtual memory map which maps the memory for the running processes(page 169, 190-192), and the event identified as one of the events to be handled by the isolated execution mode is an event that is to be handled by that process. (page 172)

Coulouris et al. does not explicitly disclose

- Maintaining a first page table map for use in an isolated execution mode and a second page table map for use in a normal execution mode.
- Dynamically swapping between the first page table map and the second page table map responsive to a change in execution mode.

Silberschatz et al. (p 270-271) discloses

- Maintaining a first page table map for use in an isolated execution mode and a second page table map for use in a normal execution mode, where the first page table map is a standard process which executes its own code in an isolated manner, and the normal execution mode is the special case of shared pages between processes.
- Dynamically swapping between the first page table map and the second page table map responsive to a change in execution mode, where processes are isolated execution modes and changing from one execution mode to another would involve a context switch from one process that doesn't use shared pages to another that does. P. 92 (processes)

Silberschatz et al. (p 270-271) discloses that there is an advantage to sharing common code, particularly in the context of a time-sharing environment, and that reentrant shared code can result in a significant savings of total memory space. P. 271 (paragraph 2)

It would have been obvious to one of ordinary skill in the art at the time of invention to use the shared code processes of Silberchatz et al. with the isolated execution processes of Coulouris et al. in order to allow for significant savings in memory while still retaining the logical boundaries of the process to allow for managed concurrent execution.

In reference to claim 2:

(Coulouris et al. Section 6.3 Processes and Threads) discloses the method of claim 1 further comprising:

- Identifying if the event is one of a class of events to be handled in the isolated execution mode, where the isolated execution mode is a processor running a secure process (Page 168), and the event is one of an event or events that might be handled by that process, where threads within a process have their own software interrupt handling mechanisms
- Handling the event using the first page table map if the event is identified as one of the class of events to be handled in the isolated execution mode, where the first page table map is the virtual memory map which maps the memory for the running processes(page 169, 190-192), and the event identified as one of the events to be handled by the isolated execution mode is an event that is to be handled by that process. (page 172)
- Wherein identifying comprises indexing into a lookup table with a exception vector of the event, where the identifying of the interrupt comprises indexing the disclosed lookup table Silberschatz et al. page (404) with the interrupt or "exception" vector page (403) & Silberschatz et al. page (402-404)

In reference to claim 3:

Coulouris et al. and Silberschatz et al. discloses the method of claim 1 wherein dynamically swapping comprises:

- Loading a set of control registers selected based on an exception vector of the event, where a set control registers may be found with the data loaded from the interrupt descriptor table registers in the case of an event, where the control registers are the memory addresses of specialized interrupt handlers which are controlled by the event (exception) table. Silberschatz et al. page (402-404)

In reference to claim 4:

Coulouris et al. and Silberschatz et al. fail to explicitly disclose the method of claim 3 wherein the set of control registers comprises:

- A global descriptor table register
- An interrupt descriptor table register
- A page table map base address register.

The examiner takes official notice that a global descriptor table register and an interrupt descriptor table register were well known in the art at the time of the invention. In particular a GDTR and an IDTR are registers that contain entries which associate each interrupt or exception identifier with a descriptor for the set of instructions that are to service the event.
Both of these registers are disclosed in a number of processors and processor programming manuals include the well known 80386 Programmer Reference Manual.

It would have been obvious to one of ordinary skill in the art at the time of invention to have a GDT register and an IDT register, so that processor knows which set of instructions to use to respond to a particular event.

In reference to claim 5:

Coulouris et al. and Silberschatz et al. discloses the method of claim 1 wherein maintaining comprises:

- Mirroring a page table base address register.
- Mirroring a memory map is not explicitly disclosed however,

Silberschatz et al.(page 445) discloses a RAID organization called mirroring in which the whole disk is duplicated. While costly, the advantages of this allow reading that is twice as fast. Silberschatz et al(p. 289) also discloses that memory maps, page tables, and processes may be placed on the actual hard disk itself in virtual memory. Silberschatz et al. discloses on p. 293, Figure 9.3 that page tables and memory maps for the memory may be stored in the actual hard disk.

The mirroring a hard disk containing virtual memory on it as disclosed by Silberschatz et al. inherently discloses

- Mirroring a page table base address register.
- Mirroring a memory map is not explicitly disclosed however,

In reference to claim 6:

(Coulouris et al. Section 6.4 Naming and Protection) discloses the method of claim 1 further comprising:

Defining a set of events that should be handled in isolated execution mode, where the set of events that should be handled by the isolated execution mode are the set of events that should be handled by a particular running process, selected by the server.

In reference to claim 7:

(Coulouris et al. Section 10.4 Distributed Coordinarion) discloses the method of claim 6 wherein the set of events to be handled in the isolated execution mode comprises:

machine check events and clock events, where the machine and clock events involve the synchronization of system clocks in a distributed system.

In reference to claim 8:

Coulouris et al. discloses the method of claim 2 wherein handling comprises:

- Determining if a current mode is the isolated execution mode, where the current mode is determined if it is in isolated execution mode, if it is determined that an isolated process is currently running. (Section 6.4 Naming and Protection)
- Loading a set of control registers with values corresponding to the first page table map if the current mode is not the isolated execution mode and the event is one of the class, where the set of control registers are loaded which contain the descriptor for the set of instructions needed to handle the current event, if it is found that the event is not to be handled by the current running process, but by another process. (Section 6.4 Naming and Protection)
- Dispatching an exception vector after the loading is complete, where the exception vector for the event is be dispatched once the new process capable of handling the event is loaded or switched to. (Section 6.4 Naming and Protection) & Figure 6.12

Claim 9 is rejected for the same reasons as claim 5, where a selection unit to select which page table map is applied responsive to receipt of an event is disclosed by (Section 6.4, Figure 6.12) Based on Applicant's arguments, the Examiner will clarify this position.

Claim 9 recites these first two limitations:

A first storage location storing control data for a first page table map;

A second storage location storing control data for a second page table map.

These two elements were previously rejected under the same basis as used for claim 5. That is, RAID mirroring comprises mirroring two hard drives, complete with the contents of the operating system and virtual memory embedded. Within this virtual memory, as Silberschatz has disclosed, is the control data for a page table map. Through hard disk mirroring, a second copy of the page table map would be inherent. The Examiner for the purposes of this rejection has called this the "second page table map"

As for the final limitation which recites: a selection unit to select which page table map is applied responsive to receipt of an event, the Examiner has cited Coulouris, Section 6.4 figure 6.12 which shows the server performing an event lookup to handle the request.

Claim 10 is rejected for the same reasons as claim 9 in that a multiplexer is merely a device, software or hardware which decides between two or more selections. The step performed in claim 10 is identical to the step performed by the selection unit in claim 9.

As per claim 11, the Examiner did not explicitly address this because he believed these limitations were understood to be present and previously addressed by the rejection of claim 9.

Claim 11 recites the apparatus of claim 9 wherein the first storage location contains a base address for the first page table map and the second storage location contains a base address for the second page table map. However, any page table map necessitates a storage location for it, as well as a base address for which the page table map starts. The first and second page table maps are disclosed by the RAID implementation of claim 5.

In reference to claim 12:

Coulouris et al. and Silberschatz et al. disclose a platform comprising:

- A processor executing in one of normal execution mode and isolated execution mode, where the processor is inherently present and necessary to execute the instructions of a process (Coulouris et al. p. 168), and where the isolated execution mode is a standard process, while a normal execution mode comprising shared memory in nonisolation is disclosed using shared pages. Silberschatz et al. (p. 270 – 272)
- A first set of control registers to define a current memory map of the platform, where the CPU contains registers containing the process IDs and logical addresses of the process control blocks. Silberschatz et al. (p. 264, figure 8.16 and page 270, figure 8.20)

- A mapping unit to dynamically load the first set of control registers responsive to an event if the event should be handled using an alternate memory map, where the alternate memory map the sharing of reentrant code between two processes. Silberschatz et al. (p. 270 – 272), while a context switch to another process is responsive to an interrupt. Silberschatz et al. (p. 92, Figure 4.3)

In reference to claim 13:

Coulouris et al. discloses the platform of claim 12 wherein the mapping unit comprises:

- A second set of registers having a first subset corresponding to control register values for a normal execution mode memory map and a second subset corresponding to control register values for an isolated execution mode memory map, where an isolated execution mode memory map is the memory map that is contained by the virtual memory map, the kernel map for the processes, and where the normal execution mode has set of registers for a shared memory map. (Section 6.5 and Memory sharing)
- A selection unit to select between the first subset and the second subset, where the selection unit selects an alternate isolated process to perform execution if it is found necessary to handle the clients' request. (Section 6.4 and Figure 6.12)

Claim 14 is rejected for the same reasons as claim 3.

Claim 15 is rejected for the same reasons as claim 4.

Conclusion

4. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of the final action and the advisory action is not mailed under after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension pursuant to 37 CFR 1.136(A) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication from the examiner should be directed to Thomas M Ho whose telephone number is (571)272-3835. The examiner can normally be reached on M-F from 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gregory A. Morse can be reached on (571)272-3838.

The Examiner may also be reached through email through Thomas.Ho6@uspto.gov

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-2100.

Customer Service Representative Telephone: 571-272-2100 Fax: 703-872-9306

TMH

October 31st, 2005

GREG
SUPERVISORY
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